IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Steven J. Koester

Examiner: Anh D. Mai

Serial No: 10/717,279

Art Unit: 2814

Filed: November 19, 2003

Docket: YOR920030533US1 (17110)

For: SEMICONDUCTOR FIELD-EFFECT TRANSISTOR HAVING STRAINED-LAYER (Previously Amended)

Dated: July 21, 2008

Confirmation No: 7401

Commissioner of Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

DECLARATION PURSUANT TO 37 C.F.R. §1.131

Sir:

I, Steven Koester, hereby declares that:

1. I am the sole inventor of the subject matter described and claimed in the above-identified patent application.

2. Prior to October 14, 2003, which is the effective filing date of U.S. Patent No. 6,849,527 to Xiang (hereinafter "Xiang"), I had conceived and reduced to practice a semiconductor field-effect transistor device as recited by Claims 1, 2 and 4-9 of the present application. The device and method of the invention was conceived and reduced to practice in the United States at the Thomas J. Watson Research Center at Yorktown Heights, New York prior to October 14, 2003, which is the effective filing date of Xiang.

3. As evidence of the conception and reduction to practice of the semiconductor field-effect transistor device referred to in paragraph 2 prior to the effective filing date of

Xiang, annexed hereto is an Exhibit A which comprises a true photocopy of assignee's (IBM) Invention Disclosure YOR8-2002-0484, which was created prior to October 14, 2003. Exhibit A includes a Main Idea section for the Invention Disclosure, which describes a semiconductor field-effect transistor device and process for forming the semiconductor field-effect transistor device in which the device includes a first strained layer of semiconductor material formed atop a substrate, the substrate having one or more threading dislocations, misfit dislocations or crystal defects that extend continuously from a source region to a drain region at an interface between the first strained layer of semiconductor material and the substrate, and which device includes blocking impurity dopant materials selected from the group comprising: In, Pb, Sb and Sn, that partially or fully occupies each said one or more threading dislocations, misfit dislocations or crystal defects along the interface. All experiments conducted by myself and experimental data obtained while reducing the invention to practice occurred in the United States at the Thomas J. Watson Research Center at Yorktown Heights, New York prior to October 14, 2003. All names and dates have been redacted in the preparation of this Declaration.

4. I do hereby declare that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that such willful false statements may jeopardize the validity or enforceability of the patent.

7-29-08
Dated

Stephen J. Koester

Disclosure YOR8-2002-0484

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By: Steve Koester **Created On:** [redacted] 05:36:01 PM
Last Modified By: Kathy Cognatello **Last Modified On:** [redacted] 08:28:28 AM

Required fields are marked with the asterisk (*) and must be filled in to complete the form.

***Title of disclosure (in English)**

Method of reducing dislocation-induced leakage in strained Si MOSFETs.

Summary

Status	Under Evaluation
Final Deadline	
Final Deadline Reason	
Processing Location	YOR
Functional Area	(703E) 703E SILICON DEVICE AND INTEGRATION TECHNOLOGY
Attorney/ Patent Professional	Robert M Trepp/Watson/IBM
IDT Team	Wilfried Haensch/Watson/IBM; Robert M Trepp/Watson/IBM
Submitted Date	[redacted] 06:31:56 PM EDT
*Owning Division	RES
Incentive Program	
Lab	
Technology Code	To select a Technology Code, click on "Select...Technology Code" in the action bar.
PVT Score	To calculate a PVT score, click on "Patent Value Tool" in the action bar.

Inventors with a Blue Pages entry

Inventors: Steve Koester/Watson/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> Koester, Steven J.	769699	22/K4WC	862-2189	Grill, Alfred

> denotes primary contact

Inventors without a Blue Pages entry

IDT Selection

Attorney/Patent Professional: Robert M Trepp/Watson/IBM

IDT Team: Wilfried Haensch/Watson/IBM, Robert M Trepp/Watson/IBM

Response Due to IP&L: [redacted]

*Main Idea

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

MOSFETs fabricated on strained Si on SiGe heterostructures have potential for improved performance due to higher carrier mobility in the strained Si layer. The relaxed SiGe buffer layers are non-ideal, and often have high densities (> 105 cm-2) of threading dislocations. During high-temperature processing, these threading dislocations can glide forming misfit dislocations at the strained Si/SiGe interface. These threading and misfit dislocations can lead to device failure in a MOSFET if the dopants from the source and drain region segregate along the dislocation, causing a direct "pipe" from source to drain. This is especially true for n-MOSFETs since the size of the n-type dopant atoms in the source and drain (usually P and As) are larger than the p-type dopant atoms in the well region (usually B). Since larger atoms preferentially occupy the dislocation, n-MOSFETs are more likely to suffer from dislocation-related failures.

The current Invention consists of a strained-Si MOSFET with a well implant that consists of a high mass atom (e.g. In for p-well, or Sb for n-well) to preferentially occupy the dislocation site and therefore prevent the segregation of dopants from the source and drain region. The advantage of using this invention is that it allows devices that are immune to dislocaiton-related failures, and therefore more robust to processing and material variations. This Invention relaxes the requirement for reducing the threading dislocation density in SiGe buffers, since the devices will be operable despite the presence of a finite number of dislocations.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?

A schematic diagram of a strained Si on relaxed SiGe n-MOSFET with a dislocation-related short is shown in Fig. 1. This figure shows a threading dislocation that protrudes up from the substrate, glides along the Si/SiGe interface and then terminates at the surface. The dopants from the source and drain can segregate along the dislocation, and if the gate length is sufficiently short, join together to form a leakage path between source and drain. In a conventional device, the source and drain dopants (As and P) preferentially occupy the dislocation, because they are larger than the well dopant (B). Fig. 2 shows one embodiment of the current invention, where the strained Si n-MOSFET utilizing a well dopant (in this case In) that is larger than the source and drain dopants. The In could be implanted at the same time as the deeper B well implant, and should have a peak concentration near the strained Si/SiGe interface. The In implant energy and dose could be adjusted so that the device threshold is not impacted by the use of a different dopant. In this case, the the In preferentially occupies the dislocation site, preventing As and P segregation along the dislocation, and thus preventing device failure.

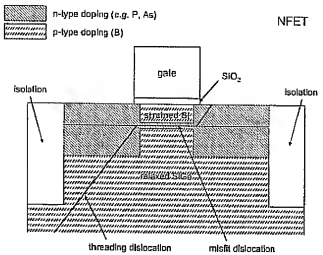

Fig. 1

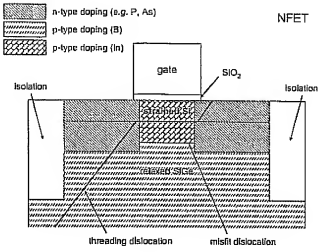

Fig. 2

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?
To my knowledge, this problem has not been identified outside of IBM, though it is generally believed that dislocations could lead to device failure. The basic solution suggested in the literature is to reduce the density of original threading dislocations. However, this could be very difficult, since dislocations are necessray to relax SiGe layers grown on Si, and even the best layers reported to date still have 1e-5 cm-2 dislocations, which could still pose significant problems for the manufacturability of this technology. The current inventions suggests a way of simply reducing the electrical activity of the dislocations, thereby allowing the device to function even in the presence of a finite number of dislocations.

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.
None.

***Critical Questions (Questions 1-9 must be answered in English)**

***Question 1**
On what date was the invention workable? 09/01/2002 **Please format the date as MM/DD/YYYY**
(Workable means i.e. when you know that your design will solve the problem)

***Question 2** ○ Yes ● No
Is there any planned or actual publication or disclosure of your invention to anyone outside IBM?
If yes, Enter the name of each publication or patent and the date published below.
Publication/Patent:
Date Published or Issued:
Are you aware of any publications, products or patents that relate to this invention? ○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below.
Publication/Patent:
Date Published or Issued:

***Question 3** ○ Yes ● No
Has the subject matter of the invention or a product incorporating the invention been

sold, used internally in manufacturing, announced for sale, or included in a proposal?
Is a sale, use in manufacturing, product announcement, or proposal planned? ○ Yes ◉ No

If Yes, identify the product if known and indicate the date or planned date of sale, announcements, or proposal and to whom the sale, announcement or proposal has been or will be made.

Product:
Version/Release:
Code Name:
Date:
To Whom:

If more than one, use cut and paste and append as necessary in the field provided.

*Question 4 ○ Yes ◉ No
Was the subject matter of your invention or a product incorporating your invention used in public, e.g., outside IBM or in the presence of non-IBMers?
If yes, give a date. Please format the date as MM/DD/YYYY

*Question 5 ○ Yes ◉ No
Have you ever discussed your invention with others not employed at IBM?
If yes, identify individuals and date discussed. Fill in the text area with the following information, the names of the individuals, the employer, date discussed, under CDA, and CDA #.

*Question 6 ○ Yes ◉ No ○ Not sure
Was the invention, in any way, started or developed under a government contract or project?
If Yes, enter the contract number

*Question 7 ○ Yes ○ No ◉ Not Sure
Was the invention made in the course of any alliance, joint development or other contract activities?
If Yes, enter the following:

Name of Alliance, Contractor or Joint Developer
Contract ID number
Relationship contact name
Relationship contact E-mail
Relationship contact phone

*Question 8 ○ Yes ◉ No
Have you, or any of the other inventors, submitted this same invention disclosure or similar invention disclosure previously?
If Yes, please provide disclosure number below:

*Question 9 ○ Yes ◉ No
Are you, or any of the other inventors, aware of any related inventions disclosures submitted by anyone in IBM previously?
If Yes, please provide the docket or disclosure number or any other identifying information below:

Question 10

What type of companies do you expect to compete with inventions of this type? *Check all that apply.*

- ☐ Manufacturers of enterprise servers
- ☐ Manufacturers of entry servers
- ☐ Manufacturers of workstations
- ☐ Manufacturers of PC's
- ☐ Non-computer manufacturers
- ☐ Developers of operating systems
- ☐ Developers of networking software
- ☐ Developers of application software
- ☐ Integrated solution providers
- ☐ Service providers
- ☐ Other (Please specify below)

Manufacturers of high-performance integrated circuits (Intel, TSMC, AMD) and companies developing SI/SiGe-related intellectual property (Amberwave)

Question 11

If the invention relates to a product or service that is outside the scope of your business unit, please recommend IBM business unit(s), IBM location(s) or individual(s) within IBM that you think would provide a good evaluation of your invention:

Patent Value Tool (Optional - this may be used by the inventor and attorney to assist with the evalua

(The Patent Value tool can be used by the inventor(s) to determine the potential licensing value of your invention.)

Market

What is the anticipated annual market size (in dollars) that will be captured by your invention?

CLAIMS

Question 1 - How new is the technical field?

Question 2 - How central is the invention to the product(s) which might be expected to contain the invention?

Question 3 - What is the scope of the claim?

PORTFOLIO NEED

What are the portfolio needs in the area of your invention?

EXPLOITATION & ENFORCEMENT

Question 1 - How easily can the use of the invention by a competitor be detected?

Question 2 - How easily can the use of the invention be avoided by a competitor?

BUSINESS VALUE

Question 1 - What percentage of the companies producing products in the field of this invention might use this invention?

Question 2 - What is the value of this patent to current or anticipated Alliance Activity between IBM and other companies?

Question 3 - What is the value of this patent to current or anticipated Technology Transfer Activity between IBM and other companies?

Question 4 - Does it result in prestige to IBM?

Post Disclosure Text & Drawings
Enter any additional information relating to this disclosure below:

(Form Revised 12/17/97)